The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte JEFFEREY S. MAILLOUX, KEVIN J. RYAN, TODD A. MERRITT, AND BRETT L. WILLIAMS

Appeal No. 2004-0414
Application 08/984,560

ON BRIEF

Before THOMAS, BARRY and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 11-21 and 59-71.

Representative claim 11 is reproduced below:

11. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing schemes and said patterned addressing scheme is selected.

The following reference is relied on by the examiner:

Manning	5,610,864	Mar. 11, 1997 (filing date Feb. 10, 1995)

Claims 11-21 and 59-71 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Manning. Appellant argues and the examiner makes reference at various portions of the answer to an inadvertent reliance upon 35 U.S.C. § 102(b) as the basis to reject the claims on appeal rather than upon 35 U.S.C. § 102(e). To expedite our consideration of the issues on this appeal, we consider the rejection in the same manner.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for appellants' positions, and to the answer for the examiner's positions.

OPINION

We reverse.

Each of independent claims 11, 59, 60, 61, 62, 65, 68 and 70 variously recite control logic for selecting between a patternless addressing scheme and a patterned addressing scheme

or selecting between a burst or a pipelined mode or selecting between an unpatterned pipelined and a patterned burst data pattern mode of operation. Correspondingly, each of these independent claims also requires the feature of switching circuitry which performs the switching of respective first and second pathways depending on which of the earlier recited addressing schemes is selected.

It goes without saying that those independent claims (59, 60, 61 and 70) that recite specifically selecting between a pipelined or a burst mode of operation are the most specific claims. On the other hand, the remaining independent claims (claims 11, 62, 65 and 68) more broadly recite the same features in a corresponding manner as to patternless and patterned addressing schemes. It is noted that the discussion at specification page 30 beginning at line 5 and at specification page 33 beginning at line 13 clearly indicates to the artisan that a patternless addressing scheme is only taught in the context of a pipelined mode of operation and that a patterned addressing scheme is only taught in a corresponding burst mode of operation.

With these considerations in mind, our study of Manning leads us to agree with appellant's assessment of this reference generally set forth in the paragraph bridging pages 3 and 4 of the principal brief on appeal. The examiner's position primarily relies upon Manning's Figure 1 as well as portions of columns 5-7. Column 5, lines 43-46 merely indicates that pipelined architectures exist as other types of memory architectures that may be applicable to the current disclosure in Manning, yet no details are supplied in any other portion of the reference to suggest the specific applicability of the burst mode operability of Manning's memory to a pipelined architecture, specifically as to how it would be implemented. The teachings at column 5, lines 43-62, in context, merely appear to teach the conceptual applicability of burst mode architectures to pipelined architectures but not presenting any further circuits in the remaining parts of the specification of Manning applicable to pipelined architectures.

Various modes are taught at column 6, lines 14-34 and column 7, lines 29-54 as relied upon by the examiner. These various modes, however, do not teach any switchability between a burst mode and a pipelined mode of operation as required by each of the

claims on appeal. We therefore agree with appellant's observation at the top of page 7 of the principal brief on appeal that "Manning never discusses the ability to switch or select between burst and pipelined modes of operation, or patternless and patterned addressing schemes, as claimed by the Appellants."

In order for us to sustain the examiner's rejection under 35 U.S.C. § 103, we would need to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejections. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). This we decline to do.

Our reviewing court has made it clear in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997), that rejections must be supported by substantial evidence in the administrative record and that where the record is lacking in evidence, this Board cannot and should not resort to unsupported speculation. As indicated in Lee, 277 F.3d at 1343-44, 61 USPQ2d at 1433-34, the examiner's finding of whether there is a teaching, motivation or suggestion to combine the teachings of the applied references must not be resolved based on "subjective belief and unknown authority," but must be "based on objective evidence of record."

The examiner's responsive arguments portion of the answer beginning at page 5 merely repeats the initial reliance in the

statement of the rejection on certain portions of columns 5-7 of Manning. As indicated earlier, these portions of Manning clearly fall short of indicating to us the anticipatory nature of the subject matter of the claims on appeal at least as applied to pipelined memory schemes. Plainly, Manning does not explain and certainly does not show in Figure 1 of his patent switching circuitry to switch between plural pathways between a pipelined/patternless addressing scheme and a burst/patterned addressing scheme, which is the essential argument provided in the brief and reply brief by appellants. More specifically, Manning does not further develop the general statement of applicability at columns 5, lines 43-46 of his invention being usable with pipelined architectures such as to explain how a plurality of memory-type operations may occur in an overlapping manner or processed simultaneously in a manner consistent in the art and recognized to be necessary for a pipelined memory accessing scheme.

Therefore, Manning alone, within 35 U.S.C. 102(b) or § 102(e), without additional evidence, cannot be fairly said to anticipate the subject matter of each independent claim on appeal. As such, the rejection of the respective dependent claims must be reversed as well.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 102 is reversed.

REVERSED

James D. Thomas)
Administrative Patent Judge)
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)
Lance Leonard Barry)
Administrative Patent Judge) BOARD OF PATENT
) APPEALS AND
) INTERFERENCES
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Stuart S. Levy)
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